Exception Design of Kabeta

# Exception Summary

## Introduction

Refer to *Section 6. Extensions for Exception Handling* in *MIT β Documentation*.

## Supported Exceptions

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Type** | **Source** | **Exc. Vector** |
| Reset | Interrupt | RST Pin | 8000\_0000 |
| System Service | Trap | RR-Stage | 8000\_0004 |
| Illegal Instruction | Fault | RR-Stage | 8000\_0008 |
| Invalid I-Address | Fault | IF-Stage | 8000\_000C |
| Invalid D-Address | Fault | MX-Stage | 8000\_0010 |
| Invalid Operation | Fault | EX-Stage | 8000\_0014 |
| External Interrupt | Interrupt | IRQ Pin | 8000\_0018 |
| (Reserved) | (N/A) | (N/A) | 8000\_001C |

Note: The MSBs of exception vectors indicate that the Supervisor bit will be set when executing the exception handlers.

## Interrupt Enable & Disable

All interrupts except Reset are disabled while executing the exception handler, i.e. in Supervisor mode.

## Double Fault

If another fault occurs while executing the fault handler, the processor will halt.

# Implementation Details

## Reset Processing

Reset all Instruction Registers and all Exception Registers, set ExcAddr = reset exception vector, and select ExcAddr as next PC value. Synchronization of external RST signal is necessary.

## Trap and Fault Processing

When a trap or fault occurs, cancel the instruction which has caused the exception and the later instructions in the pipeline, set the exception status, and jump to exception handler.

## Interrupt Processing

When an interrupt occurs, cancel the instructions later than MX-Stage, set the exception status, and jump to exception handler.